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Deepak Mehta et al.

US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM US-P	Hits 2	Search String 6,282,131.pn.	06 USPAT, EPO; JPO; DERWENT; IBM
(memory nead instancest) with compliable (memory nead instancest) with compliable (memory nead instancest) with (data nead pointst) or data) (memory nead complicits) with (data nead pointst) or data) (memory nead complicits) with (data nead pointst) or data) (memory nead complicits) with (data nead pointst) or data) (memory nead complicits) with (data nead pointst) or data) (memory nead complicits) with (data nead pointst) or data) (memory nead complicits) with (data nead pointst) or data) (memory nead complicits) with (data nead pointst) or data) (memory nead complicits) with (data nead pointst) or data) (memory with (memory with (memory with (memory nead instancest)) (memory nead instancest) with (memory nead instancest)) (memory nead instancest) (memory nead	2 0	(memory near2 compiler\$1) with (memory near2 instance\$1) (memory near2 compiler\$1) with charcaterization	USPAT; EPO; JPO; DERWENT; IBM_ USPAT; EPO; JPO; DERWENT; IBM_
(memory near2 compiles 5) with (pata near2 points 1) or data) (memory near2 compiles 5) with (pata near2 points 1) or data) (memory near2 compiles 5) with (pata near2 points 1) or data) (memory near2 compiles 5) with (pata near2 points 1) or data) (memory near2 compiles 5) with (pata near2 points 1) or data) (memory near2 compiles 5) with (pata near2 points 1) or data) (memory near2 tector 5) (memory with (MUX near2 fector 51) (s) and (memory with (MUX near2 fector 51) (s) and (memory with (MUX near2 fector 51) (s) and (memory with (memory near2 instance 51) (s) and (memory with (memory near2 instance 51) (s) and (memory near2 fector 51) (s) and (memory near2 compiles 51) with fector 620 (memory near2 compiles 51) with fector 620 (memory near2 instance 51) with (memory near2 fector 51) (memory near2 instance 51) with (memory near2 compiles 51) with (memory near2 compiles 51) with (memory near2 compiles 51) with (memory near2 instance 51) with (memo	5	(memory near2 instance\$1) with compilable	USPAT; EPO; JPO; DERWENT; IBM
Interiory nead complerefs to with (data nead 2 points) or data) US-PGPUB, USPAT, EPO, PO, DERWENT, US-PGPUB, USPAT, EPO, PO, DERWENT, SO are Sor or	81	(memory near2 instance\$1) with (parameter\$1 or parametric)	USPAT; EPO; JPO; DERWENT; IBM
(memory near2 compiles \$1) with (data near2 point\$1) or data) SS and (memory with (MUX near2 factor\$1)) SS and (memory with (mux near2 factor\$1)) SS and (memory with (mux near2 factor\$1)) SS and (memory with (manory near2 factor\$1)) SS and (congruent near2 (memory near2 factor\$1)) SS and (congruent near2 (memory near2 instancs\$1)) SS and (memory with (memory near2 instancs\$1)) SS and (memory with (memory near2 instancs\$1)) SS and (memory near2 factor\$1) SS and (memory near2 factor\$1) with instancs\$1) SS and (memory near2 factor\$1) with instancs\$1) SS and (memory near2 factor\$1) with instancs\$1) SS and ((memory near2 compiler\$1) with instancs\$2) SS and ((memory near2 compiler\$1) with (memory near2 compiler\$1) with (memory near2 compiler\$1) with (memory near2 instancs\$1) with	1628	(memory near2 instance>1) with ((data near2 point>1) or data) (memory near2 compiler\$1) with (parameter\$1 or parametric)	USPAT; EPO; JPO; DERWENT;
9 S2 or \$4 or \$5 or \$6 or \$7 or \$8 9 and (memory with (MLX near2 factor\$1)) 9 and (congruent with (memory near2 instance\$1)) 9 and (memory near2 factor\$1) with interpolat\$3) 9 and (memory near2 compiler\$1) with characterization 1	198	(memory near2 compler\$1) with ((data near2 point\$1) or data)	USPAT; EPO; JPO; DERWENT;
S9 and (memory with (MUX near2 factor\$1) S9 and (memory with (memory near2 instance\$1) S9 and (memory with (memory near2 instance\$1) S9 and (congruent mear2 factor\$1) S9 and (congruent with (memory near2 instance\$1) S9 and (memory near2 tentor\$1) near2 time) S9 and (memory near2 time) S9 and (memory near2 time) S9 and (memory near2 instance\$1) S9 and (memory near2 instance\$1) with (ROM or (istatic or dynamic) near2 RAM) or EPROM is USPAT; EPO; JPO; DERWENT; S9 and (memory near2 instance\$1) with therholog\$3 S9 and (memory near2 instance\$1) with technolog\$3 S9 and (memory near2 compiler\$1) with simulet\$3 S9 and (memory near2 compiler\$1) with technolog\$3 S9 and (memory near2 compiler\$1) with simulet\$3 S9 and (memory near2 compiler\$1) with characterization S9 and (memory near2 compiler\$1) with characterization S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and (memory near2 point\$1) or data) S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and S92 or S93 or S93 or S9	1880	S2 or S4 or S5 or S6 or S7 or S8	USPAT, EPO, JPO, DERWENT,
Sa and (minory with (parametric near2 dataset\$1) or dataset\$1) Sa and (congruent near2 (memory near2 dataset\$1) or dataset\$1) Sa and (congruent near2 (memory near2 dataset\$1) Sa and (congruent near2 (memory near2 instance\$1)) Sa and (congruent with (memory near2 instance\$1)) Sa and (scale near2 factor\$1) Sa and (memory near2 tuning) Sa and (memory near2 tuning) Sa and (memory near2 instance\$1) with (ROM or (static or dynamic) near2 RAM) or EPROM US-PGPUB. USPAT; EPO; JPO; DERWENT; SP and (Imemory near2 instance\$1) with (ROM or (static or dynamic) near2 RAM) or EPROM US-PGPUB. USPAT; EPO; JPO; DERWENT; SP and (Imemory near2 instance\$1) with interpolat\$3) Sa and ((memory near2 compiler\$1) with interpolat\$3) Sa and ((memory near2 compiler\$1) with simulat\$3) Sa and ((memory near2 compiler\$1) with characterization (memory near2 compiler\$1) with characterization (memory near2 compiler\$1) with characterization (memory near2 instance\$1) with (memory near2 compiler\$1) or data) US-PGPUB: USPAT; EPO; JPO; DERWENT; (memory near2 instance\$1) with (memory near2 populate) uspat; (memory near2 compiler\$1) with (memory near2 popul	_	ear21	USPAT; EPO; JPO; DERWENT;
S9 and (congruent near (parametric near2 dataset\$1)) or dataset\$1)) S9 and (congruent near2 (memory near2 instance\$1)) S9 and (congruent near2 factor\$1) S9 and (congruent with (memory near2 instance\$1)) S9 and (congruent with (memory near2 instance\$1)) S9 and (congruent with (memory near2 instance\$1)) S9 and (memory near2 factor\$1) near2 time)) S9 and (memory near2 timing) S9 and (memory near2 factor\$1) with interpolat\$3) S9 and (memory near2 compiler\$1) with technolog\$2) S9 and (memory near2 instance\$1) with (data near2 point\$1) or data) S9 and (memory near2 instance\$1) with (data near2 point\$1) or data) S9 and (memory near2 instance\$1) with (data near2 point\$1) or data) S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and (memory near2 compiler\$1) with (data near2 point\$1) or data) S9 and S9 or S9	-	S9 and (MUX near2 factor\$1)	USPAT; EPO; JPO; DERWENT;
S9 and (congruent near2 (nemony near2 instance\$1)) S9 and (congruent the firm from younged instance\$1)) S9 and (congruent with (memory near2 instance\$1)) S9 and (scale near2 factor\$1) S9 and (memory near2 timing) S9 and (memory near2 compiler\$1) with interpolat\$3) S17 and S21 S18 and S21 S18 and S21 S18 and S21 S19 and S21 S19 and S21 S19 and S21 S19 and S21 S10 or S11 or S12 or S23 or S24 or S25 or S26 or S27 or S28 or S2 or S26 or S27 or S28 or S26 or S27 or S28	7	S9 and (memory with ((parametric near2 dataset\$1) or dataset\$1))	USPAT; EPO; JPO; DERWENT;
S9 and (congruent with (memory neat2 instance\$1)) S9 and (congruent with (memory neat2 instance\$1)) S9 and (cacle neat2 factor\$1) S9 and (scale neat2 factor\$1) S9 and (scale neat2 factor\$1) S9 and (memory neat2 training) S9 and (memory neat2 instance\$1) with interpolat\$3) S9 and (memory neat2 instance\$1) with interpolat\$3) S9 and (memory neat2 instance\$1) with interpolat\$3) S9 and (memory neat2 compiler\$1) with technolog\$3) S9 and (memory neat2 compiler\$1) with characterization (memory neat2 compiler\$1) with characterization (memory neat2 compiler\$1) with (memory neat2 instance\$1) with (memory neat2 point\$1) or data) (memory neat2 compiler\$1) with (memory neat2 point\$1) or data) (memory neat2 compiler\$1) with (memory neat2 poin\$2) or data) (memory neat2 compiler	0	S9 and (congruent near2 (memory near2 instance\$1))	USPAT; EPO; JPO; DERWENT;
S9 and (scale near2 factor\$1) S9 and (scale near2 tactor\$1) near2 interpolat\$3) S9 and (iscale near2 tactor\$1) near2 time) S9 and (iscale near2 tactor\$1) near2 time) S9 and (iscale near2 factor\$1) with interpolat\$3) S9 and (iscale near2 factor\$1) with interpolat\$3) S9 and (iscale near2 factor\$1) with interpolat\$3) S9 and (iscale near2 compiler\$1) with interpolat\$3) S9 and (immony near2 compiler\$1) with terholog\$3) S9 and (immony near2 compiler\$1) with (parameter\$1 or parametric) S9 and (immony near2 instance\$1) with (parameter\$1 or parametric) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 instance\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (or data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (or data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) wit	0	S9 and (congruent with (memory near2 instance\$1))	USPAT; EPO; JPO; DERWENT;
S9 and ((scale near2 factor\$1) near2 interpolat\$3) S9 and (memory near2 tining) S9 and (memory near2 instance\$1) with (ROM or ((static or dynamic) near2 RAM) or EPROM US-PGPUB; USPAT; EPO; JPO; DERWENT; S17 and S18 S9 and (memory near2 instance\$1) with interpolat\$3) S9 and (memory near2 compiler\$1) with simulat\$3) S9 and (memory near2 compiler\$1) with technolog\$3) S9 and (memory with technolog\$3) with ("10" or "0.8" or "0.8" or "0.2")) S9 and (memory with technolog\$3) with ("10" or "0.8" or "0.8" or "0.2")) S9 and (memory with technolog\$3) with ("10" or "0.8" or "0.8" or "0.2")) S9 and (memory near2 compiler\$1) with technolog\$3) S9 and (memory near2 compiler\$1) with (memory near2 instance\$1) with (memory near2 point\$1) or data) S10 or S10 or S10 or S20 o	16	S9 and (scale near2 factor\$1)	USPAT; EPO; JPO; DERWENT;
S9 and (memory near2 timig) S9 and (memory with ((access or cycle) near2 time)) S9 and (memory with (access or cycle) near2 time)) S9 and (memory near2 instance\$1) with (ROM or ((static or dynamic) near2 RAM) or EPROM US-PGPUB, USPAT; EPO; JPO; DERWENT; S9 and ((memory near2 factor\$1) with interpolat\$3) S9 and ((memory near2 factor\$1) with interpolat\$3) S9 and ((memory near2 compiler\$1) with simulat\$3) S9 and ((memory near2 compiler\$1) with simulat\$3) S9 and ((memory near2 compiler\$1) with technolog\$3) S9 and ((memory near2 compiler\$1) with technolog\$3) S9 and ((memory near2 compiler\$1) with characterization (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) US-PGPUB, USPAT; EPO; JPO; DERWENT; S9 and ((memory near2 compiler\$1) with (data near2 point\$1) or data) US-PGPUB, USPAT; EPO; JPO; DERWENT; S9 and ((memory near2 compiler\$1) with (data near2 point\$1) or data) US-PGPUB, USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with ((data near2 point\$1) or data) US-PGPUB, USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with ((data near2 point\$1) or data) US-PGPUB, USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with ((data near2 point\$1) or data) US-PGPUB, USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with ((data near2 point\$1) or data) US-PGPUB, USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with ((data near2 point\$1) or data) US-PGPUB, USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with ((data near2 point\$1) or data) US-PGPUB, USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with ((data near2 point\$1) or data) US-PGPUB, USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with ((data near2 point\$1) or data) US-PGPUB, USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with ((data near2 point\$1) or data)	0		USPAT; EPO; JPO; DERWENT;
S9 and (memory with ((access or cycle) near2 time)) S17 and S18 S18 and (MUX-4 or MUX-8 or MUX-32) S19 and (MUX-4 or MUX-8 or MUX-16 or MUX-32) S19 and (MUX-4 or MUX-8 or MUX-16 or MUX-32) S19 and ((memory near2 instance\$1) with interpolat\$3) S17 and S21 S17 and S21 S17 and S21 S18 and S21 S18 and S21 S19 and (incemory near2 compiler\$1) with simulat\$3) S17 and S21 S18 and S21 S19 and (incemory near2 compiler\$1) with simulat\$3) S17 and S21 S18 and S21 S19 and (incemory near2 compiler\$1) with simulat\$3) S17 and S21 S18 and S21 S19 and (incemory near2 compiler\$1) with characterization S19 and (incemory near2 compiler\$1) with characterization S19 and (incemory near2 compiler\$1) with characterization Cmemory near2 compiler\$1) with (parameter\$1 or parametric) Cmemory near2 compiler\$1) with (parameter\$1 or parametric) Cmemory near2 instance\$1) with (parameter\$1 or parametric) Cmemory near2 compiler\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; Cmemory near2 instance\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; Cmemory near2 instance\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; Cmemory near2 compiler\$1 with ((data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; Cmemory near2 compiler\$1 with ((data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; Cmemory near2 compiler\$1 with ((data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; Cmemory near2 compiler\$1 with ((data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; Cmemory near2 compiler\$1 with ((data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; Cmemory near2 compiler\$1 with ((data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; CMEMORY near2 compiler\$1 with ((data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; CMEMORY near2 compiler\$1 with ((data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; CMEMORY DERWENT; CMEMORY DERWENT; CMEMORY DERWENT	109	S9 and (memory near2 timing)	USPAT; EPO; JPO; DERWENT;
S17 and S18 S9 and (MUX-4 or MUX-8 or MUX-32) S9 and (Imemory near2 instance\$1) with interpolat\$3) S17 and S21 S17 and S21 S18 and S21 S18 and S21 S18 and S21 S19 and (imemory near2 compiler\$1) with simulat\$3) S9 and (imemory near2 compiler\$1) with technolog\$3) S9 and (imemory near2 compiler\$1) with characterization (imemory near2 compiler\$1) with characterization (imemory near2 compiler\$1) with (memory near2 instance\$1) (imemory near2 compiler\$1) with (memory near2 instance\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data) (imemory near2 compiler\$1) with (data near2 point\$1) or data)	250	S9 and (memory with ((access or cycle) near2 time))	USPAT; EPO; JPO;
S9 and (MUX-4 or MUX-8 or MUX-16 or MUX-32) S9 and (memory near2 instance\$1) with (ROM or ((static or dynamic) near2 RAM) or EPROM US-PGPUB; USPAT; EPO; JPO; DERWENT; S9 and ((scale near2 factor\$1) with interpolat\$3) S17 and \$21 S17 and \$21 S18 and (S21 S17 and \$21 S18 and (S21 S17 and \$21 S18 and (memory near2 compiler\$1) with simulat\$3) S9 and ((memory near2 compiler\$1) with technolog\$3) S9 and ((memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data)	37	S17 and S18	USPAT; EPO; JPO;
S9 and ((memory near2 instance\$1) with interpolat\$3) S17 and \$23 S9 and ((scale near2 factor\$1) with interpolat\$3) S17 and \$24 S17 and \$25 S18 and \$25 S17 and \$25 S18 and \$25 S19 and ((memory near2 compiler\$1) with technolog\$3) S19 and ((memory near2 rule\$1) or foundry-specific or process-specific or process US-PGPUB; USPAT; EPO; JPO; DERWENT; S19 or \$15 or \$	0	S9 and (MUX-4 or MUX-8 or MUX-16 or MUX-32)	USPAT; EPO; JPO;
S9 and ((scale near2 factor\$1) with interpolat\$3) S17 and S21 S18 and S22 S18 and ((memory near2 compiler\$1) with technolog\$3) S10 and ((memory near2 compiler\$1) or foundry-specific or rule-specific or process-specific or process US-PGPUB; USPAT; EPO; JPO; DERWENT; S10 or S15 or S20 or S25 or S26 or S27 or S28 or S2 or S2 or S20 or	176	S9 and ((memory near2 instance\$1) with (ROM or ((static or dynamic) near2 RAM) or EPROM	US-PGPUB; USPAT;
US-PGPUB; USPAT; EPO; JPO; DERWENT; USPAT; E	4	le near2 factor\$1) with	USPAT; EPO; JPO;
S18 and S21 S9 and ((memory near2 compiler\$1) with simulat\$3) S9 and ((memory near2 compiler\$1) with simulat\$3) S9 and ((memory near2 compiler\$1) with technolog\$3) S9 and ((memory near2 compiler\$1) with technolog\$3) S9 and ((memory with technolog\$3) with ("1.0" or "0.8" or "0.6" or "0.2")) S9 and ((memory with technolog\$3) with ("1.0" or "0.8" or "0.6" or "0.2")) S9 and ((design near2 rule\$1) or foundry-specific or rule-specific or process US-PGPUB; USPAT; EPO; JPO; DERWENT; S10 or S11 or S12 or S15 or S23 or S23 or S24 or S25 or S26 or S27 or S28 or S2 or S US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (memory near2 instance\$1) (memory near2 compiler\$1) with (memory near2 instance\$1) (memory near2 instance\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$2 or S33 or S34 or S35 or S36 S31 or S32 or S33 or S33 or S34 or S36 DERWENT;	23	S17 and S21	USPAT; EPO; JPO;
S9 and ((memory near2 compiler\$1) with simulat\$3) S9 and ((memory near2 compiler\$1) with technolog\$3) S9 and ((memory near2 compiler\$1) with technolog\$3) S9 and ((memory near2 compiler\$1) with technolog\$3) S9 and ((memory near2 compiler\$1) or "0.8" or "0.6" or "0.2") S9 and ((memory near2 rule\$1) or foundry-specific or rule-specific or process uspecific or users uspecific or users uspecific or users us	14	S18 and S21	USPAT; EPO; JPO; DERWENT;
S9 and ((memory near2 compiler\$1) with technolog\$3) S9 and ((memory near2 compiler\$1) with technolog\$3) S9 and ((memory with technolog\$3) with ("1.0" or "0.8" or "0.2")) S9 and ((memory with technolog\$3) with ("1.0" or "0.8" or "0.6" or "0.2")) S9 and ((design near2 rule\$1) or foundry-specific or rule-specific or process-specific or process US-PGPUB; USPAT; EPO; JPO; DERWENT; S10 or S11 or S15 or S19 or S22 or S23 or S24 or S25 or S26 or S27 or S28 or S2 or S US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with characterization US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (parameter\$1 or parametric) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 instance\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (data near2 point\$1) or data) US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with (data near2 point\$1) or data)	လ	S9 and ((memory near2 compiler\$1) with simulat\$3)	USPAT, EPO, JPO, DERWENT;
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S9 and ((design near2 rule\$1) or foundry-specific or rule-specific or process-specific or process-specific or process-specific or process-specific or process-specific or S10 or S12 or S15 or S19 or S22 or S23 or S24 or S25 or S26 or S27 or S28 or S2 or S US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with characterization (memory near2 compiler\$1) with compilable (memory near2 instance\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data)	-	S9 and ((memory with technolog\$3) with ("1.0" or "0.8" or "0.6" or "0.2"))	USPAT; EPO; JPO; DERWENT;
\$10 or \$11 or \$12 or \$15 or \$19 or \$22 or \$23 or \$24 or \$25 or \$26 or \$27 or \$28 or \$2 or \$US-PGPUB; USPAT; EPO; JPO; DERWENT; (memory near2 compiler\$1) with characterization (memory near2 compiler\$1) with compilable (memory near2 instance\$1) with (parameter\$1 or parametric) (memory near2 instance\$1) with (parameter\$1 or parametric) (memory near2 compiler\$1) with (parameter\$1 or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (parameter\$1 or data) (memory near2 compiler\$1) with (parameter\$1 or data) (memory near2 compiler\$1) with (parameter\$1) or data) (memory near2 compiler\$1) with (parameter\$2 or \$20 or	4	S9 and ((design near2 rule\$1) or foundry-specific or rule-specific or process-specific or process	USPAT; EPO; JPO; DERWENT;
(memory near2 compiler\$1) with characterization US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_USPAT; EPO; JPO; DERWENT; IBM_US	150	S10 or S11 or S12 or S15 or S19 or S22 or S23 or S24 or S25 or S26 or S27 or S28 or S2 or §	USPAT; EPO; JPO; DERWENT;
(memory near2 compiler\$1) with (memory near2 instance\$1)US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_USPAT; EPO; JPO; DERWENT;	7	(memory near2 compiler\$1) with characterization	USPAT; EPO, JPO, DERWENT;
(memory near2 instance\$1) with compilable (memory near2 instance\$1) with (parameter\$1 or parametric) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data)	14	(memory near2 compiler\$1) with (memory near2 instance\$1)	USPAT; EPO; JPO; DERWENT; IBM
(memory near2 instance\$1) with (parameter\$1 or parametric) (memory near2 instance\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (parameter\$1 or parametric) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (data near2 point\$1) or data) (memory near2 compiler\$1) with (parameter\$1) or data) (memory near2 compiler\$1) with (parameter\$1) or data)	10	(memory near2 instance\$1) with compilable	USPAT; EPO; JPO; DERWENT; IBM
(memory near2 instance\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with (parameter\$1 or parametric) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (S31 or S32 or S33 or S34 or S35 or S36	8	(memory near2 instance\$1) with (parameter\$1 or parametric)	USPAT; EPO; JPO; DERWENT; I
(memory near2 compiler\$1) with (parameter\$1 or parametric) (memory near2 compiler\$1) with ((data near2 point\$1) or data) (S31 or S32 or S33 or S34 or S35 or S36	1628	(memory near2 instance\$1) with ((data near2 point\$1) or data)	EPO; JPO; DERWENT; I
(memory near2 compiler\$1) with ((data near2 point\$1) or data) S31 or S32 or S33 or S34 or S35 or S36	52	(memory near2 compiler\$1) with (parameter\$1 or parametric)	
S31 or S32 or S33 or S34 or S35 or S36 USPAT; EPO; JPO; DERWENT; IBM_	198	(memory near2 compiler\$1) with ((data near2 point\$1) or data)	EPO; JPO; DERWENT; IBM
	1880	S31 or S32 or S33 or S34 or S35 or S36	EPO; JPO; DERWENT; IBM_

S38 1	S37 and (memory with (MUX near2 factor\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
		LISPAT: EDO: JDO:
	S37 and (scale near2 factor\$1)	USPAT: EPO: JPO: DERWENT: IBM USPAT: EPO: JPO: DERWENT: IBM
		USPAT; EPO; JPO; DERWENT; IBM
		USPAT; EPO; JPO; DERWENT;
S44 37		DERWENT;
		US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
		USPAT; EPO; JPO; DERWENT; I
		DERWENT;
		DERWENT;
		US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
_		DERWENT;
		US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
	_	DERWENT;
		EPO;
		DERWENT;
		US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
		US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
		US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
	S37 and (memory with ("1.0" or "0.8"	USPAT; EPO; JPO; DERWENT; IBM_
		USPAT; EPO; JPO; DERWENT; IBM
		USPAT; EPO; JPO; DERWENT; IBM_
	S55 or S58 or S59 or S60 or S61 or S62	; USPAT; EPO; JPO; DERWENT; IBM_
		; USPAT; EPO; JPO; DERWENT;
		USPAT; EPO; JPO; DERWENT; IBM
	_	; USPAT; EPO; JPO; DERWENT; IBM_
	(memory near2 instance\$1) with co	; USPAT; EPO; JPO; DERWENT;
	_	; USPAT; EPO; JPO; DERWENT; IBM_
	(memory near2 compiler\$1) with (p	; USPAT; EPO; JPO; DERWENT; IBM_
		; USPAT; EPO; JPO; DERWENT; IBM_
		, USPAT; EPO; JPO; DERWENT; IBM_
		; USPAT; EPO; JPO; DERWENT; IBM_
		; USPAT; EPO; JPO; DERWENT; IBM_
		; USPAT; EPO; JPO; DERWENT; IBM_
		; USPAT; EPO; JPO; DERWENT; IBM_
	S70 and (memory near2 timing)	USPAT; EPO; JPO; DERWENT; IBM_
	•	USPAT; EPO; JPO; DERWENT; IBM_
		USPAT; EPO; JPO; DERWENT;
		USPAT; EPO; JPO; DERWENT;
		USPAT; EPO; JPO; DERWENT; IBM_
	S75 and S78	USPAT; EPO; JPO;
S82 5	S70 and ((memory near2 compiler\$1) with simulat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

DERWENT, IBM_TDB DERWENT, IBM_TDB DERWENT, IBM_TDB DERWENT, IBM_TDB DERWENT, IBM_TDB DERWENT, IBM_TDB	VENT; IBM_TDB VENT; IBM_TDB		Abstract
USPAT; EPO; JPO; USPAT; EPO; JPO; USPAT; EPO; JPO; USPAT; EPO; JPO; USPAT; EPO; JPO; USPAT; EPO; JPO; USPAT; EPO; JPO;	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB USPAT USPAT USPAT USPAT	10/3/2006	Issue Date Current OR 20060928 714/726 20060914 365/201 20060914 365/201 20060824 702/117 20060824 365/94 20060810 717/151 20060801 717/151 20060601 711/128 20060601 711/120 20060902 365/189.05 20050516 365/189.05 20050516 711/120 20050516 711/147 20050310 717/135 20050310 717/135 20050310 717/135
S70 and ((memory near2 compiler\$1) with technolog\$3) S76 and S78 S70 and ((memory with technolog\$3) with ("1.0" or "0.8" or "0.6" or "0.2")) S70 and ((design near2 rule\$1) or foundry-specific or rule-specific or process-specific or process S86 and S79 S86 and S74 S71 or S73 or S74 or S77 or S79 or S80 or S81 or S82 or S83 or S84 or S85 or S64 or the S71 or S72 or S73 or S74 or S75 or S85 or	(memory near2 compiler\$1) or (memory near2 instance\$1) 1 and (compiler with (characteriz\$3 or characterization)) 2 and ((sampl\$3 with combination) or ((set or subset) with combination)) 2 and (select\$3 with (combination or set or subset)) 2 and (interpolat\$3 with instance) 2 and (interpolat\$3 with instance) 3 and (("black box" or "white box") near2 model) 3 or 4 or 5 or 6	Deepak Mehta et al. EAST SEARCH	Integrated circuit margin stress test system Memory compiler redundancy System and method for testing a memory ROM with a partitioned source line architecture Building a wavecache Digital method and device for transmission with reduced crosstalk Ternary cam with software programmable cache policies Electronic camera that reduces processing time by performing different processes in parallel Method and device for transmission with reduced crosstalk SIMD processor and addressing method Data communications device, data communications system, document display method with vide Access method for a NAND flash memory chip, and corresponding NAND flash memory chip, and corresponding named of generating the same Tightly coupled and scalable memory and execution unit architecture Systems and methods for using metrics to control throttling and swapping in a message process Data processor having cache memory Generation of software objects from a hardware description Reconfigurable memory arrays Design method for essentially digital systems and components thereof and essentially digital sys
S83 11 S81 19 S84 2 S85 51 S87 4 S88 23 S86 190	L1 9835 L2 46 L3 2 L4 13 L5 1 L6 1	9981954	Besults of search set S61 Document Kind Codes Title US 20060218455 A1 Integ US 20060203582 A1 Merr US 20060190208 A1 Syst US 20060190208 A1 Syst US 20060171476 A1 Digit US 20060017143 A1 Terr US 20060017143 A1 Terr US 2006001756 A1 Data US 20050149891 A1 Merr US 2005014560 A1 Tighr US 20050168398 A1 Syst US 20050108398 A1 Syst US 20050102472 A1 Data US 2005016575 A1 Gent US 20050047238 A1 Recc

20041028 711/138 20041014 711/103 20041014 365/185.29 20041014 365/185.01 2004007 365/202 20040617 703/14 20040617 703/14 20040617 703/14 20040617 703/14 20040617 703/14 20040617 703/14 20040617 703/14 20040617 703/14 20040617 703/14 20040617 703/14 20040617 703/14 20040617 703/14 20040617 703/14 20031204 707/1 20031204 707/1 20030005 265/185.29 20030005 365/185.29 20030005 365/185.29 20030124 365/200 20030128 365/186.29 20020124 365/200 200201128 365/184 20021128 365/184 20021128 365/184 200201148 365/184 20020117 714/118 20020411 714/118	
Method for use of ternary cam to implement software programmable cache policies Memory device Nonvolatile semiconductor memory device Nonvolatile semiconductor memory device Nonvolatile semiconductor memory device Nonvolatile semiconductor memory device Semiconductor memory device Memory module and method for operating a memory module in a data memory system Optimized execution of software objects generated from a hardware description Global analysis of software objects generated from a hardware description Method for composing memory on programmable platform devices to meet varied memory requi Lock-free overflow strategy for work stealing Compilable address magnitude comparator for memory array self-testing Data communications device, data communications system, document display method with vide Method, article of manufacture and apparatus for performing automatic intermodule call linkage o Method and apparatus for facilitating process-compliant layout optimization Gate array core cell for VLSI ASIC devices Method and apparatus for rectifying a stereoscopic image Write-barrier maintenance in a garbage collector Semiconductor memory device Redundancy circuit and method for replacing defective memory cells in a flash memory device Redundancy circuit and method for compilable dram Nonvolatile semiconductor memory device Timing circuit and method for redundancy implementation in a semiconductor device SRAM emulator Memory CENERCH OPERABLE WITH A SMALL-CAPACITY BUFFER MEMORY AND HAVINI Streaming memory controller Method and system for distributed testing of electronic devices Processor with cache controller	Semiconductor memory device Data processor having cache memory Nonvolatile semiconductor memory device Memory management table producing method and memory device System and method for providing adjustable read margins in a semiconductor memory Method of and apparatus for rectifying a stereoscopic image Nonvolatile semiconductor memory device Electrically-alterable non-volatile memory cell Embedded test and repair scheme and interface for compiling a memory assembly with redunda Method, article of manufacture and apparatus for performing automatic intermodule call linkage of Compilable address magnitude comparator for memory array self-testing
US 20040215893 A1 US 20040205290 A1 US 20040202019 A1 US 20040196712 A1 US 20040196712 A1 US 20040117168 A1 US 20040117167 A1 US 20040117169 A1 US 200400117169 A1 US 20040015925 A1 US 20030204676 A1 US 20030204676 A1 US 20030192013 A1 US 20030192013 A1 US 20030103779 A1 US 200300026129 A1 US 200300026129 A1 US 200200131320 A1 US 200200131320 A1 US 20020042897 A1 US 2002003881 A1	2002001303 20010048610 20010037432 20010014933 7114118 B1 7113632 B2 7099199 B2 7095076 B1 7095076 B1 7095076 B1 7095076 B1

	20060321 707/206 20060307 348/333.01 20060221 365/94 20060131 365/201 20051115 716/17 20050813 365/20 20050816 707/205	20050810 701720 20050809 365/185.2 20050517 710/22 20050510 714/42 2005020 365/63 20050125 711/129 2005011 365/185.18 20041228 711/169 20041228 711/169	20040907 365/185.08 200400608 365/185.29 20040601 716/2 20040511 365/185.2 20040323 365/233 20040339 7711/5 20040113 703/14 20031202 714/718 20030720 774/711 20030722 774/711 20030722 365/233 20030723 365/185.11 20030715 365/185.11 20030701 365/63 20030624 365/233 20030624 365/233 20030610 771/209 20030610 771/209
Memory model for a run-time environment Wordline-based source-biasing scheme for reducing memory cell leakage Memory compiler redundancy Method for use of ternary CAM to implement software programmable cache policies Partitioned source line architecture for ROM System and method for testing a memory Nonvolatile semiconductor memory device	Multi-threaded garbage collector employing cascaded memory arrays of task identifiers to impler Data communications device, data communications system, document display method with vide Methods and apparatuses for a ROM memory array having a virtually grounded line Methods and apparatuses for test circuitry for a dual-polarity non-volatile memory cell . Method for composing memory on programmable platform devices to meet varied memory requi Variable column redundancy region boundaries in SRAM Reconfigurable memory arrays.	Witterbailter in the first particular of the series of the	Electrically-alterable non-volatile memory cell Gate array core cell for VLSI ASIC devices Nonvolatile semiconductor memory apparatus Method and apparatus for facilitating process-compliant layout optimization System and method for memory characterization System and method for memory characterization Semiconductor device having a high-speed data read operation Semiconductor device having a high-speed data read operation Semiconductor test system Compilable address magnitude comparator for memory array self-testing Realtime parallel processor system for transferring common information among parallel processor Memory management table producing method and memory device Memory device generator for generating memory devices with redundancy Built-in precision shutdown apparatus for effectuating self-referenced access timing scheme Redundancy circuit and method for replacing defective memory cells in a flash memory device Data processor having cache memory System and method for increasing performance in a compilable read-only memory (ROM) SRAM emulator Optimized virtual memory management for dynamic data types Redundancy circuit and method for flash memory devices
7073033 7061794 7046561 7039756 7035129 7031866 702028	US 7016923 B2 US 7009650 B2 US 7002827 B1 US 6992938 B1 US 696044 B2 US 6944075 B1 US 6934174 B2	6928000 6928000 6895452 6895328 6853572 6850446 6848027 6842375 6836831	US 6788574 B1 US 6765245 B2 US 6745372 B2 US 6738953 B1 US 6735120 B2 US 6771092 B1 US 6678643 B1 US 667465 B2 US 6658610 B1 US 6658610 B1 US 6659619 B1 US 6659619 B1 US 6659619 B1 US 6659712 B2 US 6659712 B2 US 659712 B2

US 663504 B. Semiconductor memory device that need operation US 663504 B. Semiconductor memory device that need operation US 663507 B. Semiconductor memory device that need operation US 663507 B. Semiconductor memory device that need operation US 663507 B. Semiconductor memory device that need operation US 663507 B. Semiconductor memory device that need operation or need to semiconductor memory device to the need of the need operation of the need of the need operation or need to semiconductor memory device to the need operation of the need operation of the need of	US 6556490 B2	System and method for redundancy implementation in a semiconductor device	20030429 365/200
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	US 5644753 A		

US 5640349 A	Flash memory system	19970617 365/185.33
US 5634107 A	Data processor and method of processing data in parallel	19970527 711/111
US 555555 A	Apparatus which detects lines approximating an image by repeatedly narrowing an area of the in	19960910 382/104
US 5528552 A	Dynamic random access memory device with sense amplifiers serving as cache memory indepe	19960618 365/238.5
US 5493507 A	Digital circuit design assist system for designing hardware units and software units in a desired	19960220 703/14
US 5479374 A	Semiconductor memory device employing sense amplifier control circuit and word line control cir	19951226 365/233.5
US 5479184 A	Videotex terminal system using CRT display and binary-type LCD display	19951226 345/3.1
US 5452226 A	Rule structure for insertion of new elements in a circuit design synthesis procedure	19950919 716/18
US 5400267 A	Local in-device memory feature for electrically powered medical equipment	19950321 702/59
US 5399912 A	Hold-type latch circuit with increased margin in the feedback timing and a memory device using	19950321 327/94
US 5222029 A	Bitwise implementation mechanism for a circuit design synthesis procedure	19930622 716/18
US 5175707 A	Semiconductor memory device having a driving circuit provided in association with a high speed	19921229 365/230.06
US 5050091 A	Integrated electric design system with automatic constraint satisfaction	19910917 716/10
US 5046113 A	Method of and apparatus for detecting pattern defects by means of a plurality of inspecting units	19910903 382/147
US 4945495 A	Image memory write control apparatus and texture mapping apparatus	19900731 345/552
US 4875192 A	Semiconductor memory with an improved nibble mode arrangement	19891017 365/193
US 4845640 A	High-speed dual mode graphics memory	19890704 345/572
US 4803476 A	Video terminal for use in graphics and alphanumeric applications	19890207 345/545
US 4688182 A	Method and apparatus for generating a set of signals representing a curve	19870818 345/442
US 4686636 A	Method and apparatus for generating a set of signals representing a curve	19870811 345/442
US 4686634 A	Method and apparatus for generating a set of signals representing a curve	19870811 345/442
US 4686633 A	Method and apparatus for generating a set of signals representing a curve	19870811 345/442
US 4465349 A	Microfilm card and a microfilm reader with automatic stage positioning	19840814 353/25
US 4431007 A	Referenced real-time ultrasonic image display	19840214 600/440
US 4314331 A	Cache unit information replacement apparatus	19820202 711/133
US 4245304 A	Cache arrangement utilizing a split cycle mode of operation	19810113 711/122
US 4208716 A	Cache arrangement for performing simultaneous read/write operations	19800617 711/3
EP 647900 A1	Parameter storage space allocation.	19950412
US 7046561 B	Application specific integrated circuit chip has control block with defective memory register to str	20060516
US 7035129 B	Read only memory instance for compilation by memory compiler, decodes source line segments	20060425
US 7031866 B	Memory compiler for multi-instance memory device, generates test and repair wrapper, to gener	20060418
US 20050060500 A	Memory compiler units accessing method for generating memory related design files, involves di	20050317
	Memory e.g. ROM characterization method, involves creating hierarchically-stitched parametric I	20040518
	Timing synchronization method in memory instance, involves enabling address signals for subse	20010828
US 6249901 B	Automatic memory characterization for designing integrated circuit, involves simulating circuit ba	20010619
EP 191134 A	Display data encoding of signals representing curve - using parametric cubic polynomial functior	19860820
EP 175179 A	Signal generation method for points on curve - using compiler in form of Hermite cubic paramete	19860326

08				Abstract
erence chacked	10/3/2006	US-PGPUB US-PGPUB US-PGPUB US-PGPUB US-PGPUB US-PGPUB US-PGPUB	10/3/2006	lssue Date Current OR 20060928 714/726 20060914 365/201 20060824 702/117 20060824 365/94 20060810 717/151 20060803 375/257 20060801 711/128 20060601 711/128 20060511 455/295 20060302 711/220 2005092 365/185.33 20050519 716/3 20050519 710/22 20050519 709/225 20050512 711/147
Deepak Mehta et al.	Search String	(memory near2 compiler\$1) or (memory near2 instance\$1) 31 and (compiler with (characteriz\$3 or characterization)) 32 and (sampl\$3.CLM.) 32 and ("mux factor" or (column near2 multiplex\$3)) 32 and (memory with instance) 32 and (set or subset or combination) 32 and ("white box" or "balck box") 32 or 35 or 36 Deepak Mehta et al.	EAST SEARCH	rated circuit margin stress test system ory compiler redundancy em and method for testing a memory livith a partitioned source line architecture. In a wavecache line architecture in a wavecache all method and device for transmission with reduced crosstalk ary cam with software programmable cache policies ronic camera that reduces processing time by performing different processes in parallel od and device for transmission with reduced crosstalk. To processor and addressing method communications device, data communications system, document display method with ss method for a NAND flash memory chip, and corresponding NAND flash memory chip, sory compiler with ultra low power feature and method of use ory circuit and method of generating the same ly coupled and scalable memory and execution unit architecture sms and methods for using metrics to control throttling and swapping in a message proprocessor having cache memory.
9981954	Hits	L31 3836 L32 4 L33 0 L34 0 L35 3 L36 4 L37 0 L37 0		Results of search set S61 Document Kind Codes Title US 20060218455 A1 Integ US 20060190208 A1 Syst US 20060190208 A1 Syst US 20060179429 A1 Build US 20060171476 A1 Digit US 20060117143 A1 Tern US 20060117143 A1 Tern US 20060017756 A1 Data US 20050120818 A1 Meth US 20050149891 A1 Mem US 20050149891 A1 Data

Memory device Nonvolatile semiconductor memory device Nonvolatile semiconductor memory device Semiconductor memory device Semiconductor memory device Semiconductor memory device Memory module and method for operating a memory module in a data memory system Optimized execution of software objects generated from a hardware description Optimized execution of software objects generated from a hardware description Optimized execution of software objects generated from a hardware description Method for composing memory on programmable platform devices to meet varied memory r Lock-free overflow strategy for work stealing Compilable address magnitude comparator for memory array self-testing Compilable address magnitude comparatus for memory atticle of manufacture and apparatus for performing automatic intermodule call linka Data communications device, data communications system, document display method with Data communications device, data communications system, document display method with Data processor having cache memory Method and apparatus for rectifying a stereoscopic image Semiconductor memory device REDUNDANCY CIRCUIT AND METHOD FOR FLASH MEMORY DEVICES Semiconductor memory device REDUNDANCY CIRCUIT and method for a compilable dram Nonvolatile semiconductor memory device Timing circuit and method for a compilable dram Nonvolatile semiconductor memory device System and method for redundancy implementation in a semiconductor device Social 20201202 System and method for redundancy implementation in a semiconductor device
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Method of and apparatus for rectifying a stereoscopic image Nonvolatile semiconductor memory device Electrically-alterable non-volatile memory cell	Embedded test and repair scheme and interface for compiling a memory assembly with redu	Method, article of manufacture and apparatus for performing automatic intermodule call link: Compilable address magnitude comparator for memory array self-testing	Memory model for a run-time environment	Wordline-based source-biasing scheme for reducing memory cell leakage	Memory compiler redundancy	Method for use of ternary CAM to implement software programmable cache policies	Partitioned source line architecture for ROM	System and method for testing a memory	Nonvolatile semiconductor memory device	Multi-threaded garbage collector employing cascaded memory arrays of task identifiers to in	Data communications device, data communications system, document display internor with Methods and apparatuses for a ROM memory array having a virtually grounded line.	Methods and apparatuses for test circuitry for a dual-polarity non-volatile memory cell	Method for composing memory on programmable platform devices to meet varied memory r	Variable column redundancy region boundaries in SRAM		Write-barrier maintenance in a garbage collector	Semiconductor memory device having a resistance adjustment unit	Tightly coupled and scalable memory and execution unit architecture	Method and system for distributed testing of electronic devices	Methods and apparatuses for a ROM memory array having twisted source or bit lines	Memory cell sensing with low noise generation	Data processor having cache memory	Methods and apparatuses for maintaining information stored in a non-volatile memory cell	Independent sequencers in a DRAM control structure	Nonvolatile semiconductor memory device	Electrically-alterable non-volatile memory cell	Gate array core cell for VLSI ASIC devices	Nonvolatile semiconductor memory apparatus	Method and apparatus for facilitating process-compliant layout optimization	System and method for memory characterization	Semiconductor device having a high-speed data read operation	Semiconductor memory with multiple timing loops	Memory with vectorial access	Event based semiconductor test system
US 7113632 B2 US 7099199 B2 US 7095076 B1	7093156	US 7086044 B2 US 7073112 B2	7073033	US 7061794 B1	7046561		7035129	7031866	7020028	7016923	US 7009650 BZ	6992938	6966044	US 6944075 B1	US 6934174 B2	US 6931423 B2	US 6928000 B2	US 6895452 B1	US 6892328 B2	US 6853572 B1	US 6850446 B1	US 6848027 B2	US 6842375 B1	US 6836831 B2	6791882	6788574	US 6765245 B2	US 6747902 B2	US 6745372 B2	6738953	6735120	6711092	US 6/04834 B1	115 6678643 B1

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Memory management table producing method and memory device Memory device generator for generating memory devices with redundancy Built-in precision shutdown apparatus for effectuating self-referenced access timing scheme Redundancy circuit and method for replacing defective memory cells in a flash memory devi Data processor having cache memory System and method for increasing performance in a compilable read-only memory (ROM) SRAM emulator	Optimized virtual memory management for dynamic data types Redundancy circuit and method for flash memory devices System and method for redundancy implementation in a semiconductor device Timing circuit and method for a compilable DRAM Semiconductor memory device having high speed data read operation Low power read circuitry for a memory circuit based on charge redistribution between bitline: Compilable block clear mechanism on per I/O basis for high-speed memory	Memory controller with programmable delay counter for tuning performance based on timing Nonvolatile semiconductor memory device Nonvolatile semiconductor memory device Memory device operable with a small-capacity buffer memory and having a flash memory Automated design of digital signal processing integrated circuit Controlling burst sequence in synchronous memories System and method for increasing performance in a compilable read-only memory (ROM) Memory compiler interface and methodology	Way to compensate the effect of coupling between bitlines in a multi-port memories Architecture with multi-instance redundancy implementation Reduced latency row selection circuit and method Method for controlling several stepping motor modules with prior loading of ramp data Dynamically-tunable memory controller Hierarchical sense amp and write driver circuitry for compilable memory Self-timed clock circuitry in a multi-bank memory instance using a common timing synchron Data processor with variable types of cache memories and a controller for selecting a cache Nonvolatile semiconductor memory device Memory characterization system Fast full signal differential output path circuit for high-speed memory Centrally decoded divided wordline (DWL) memory architecture Multi-port semiconductor memory and compiler having capacitance compensation Method and apparatus for a nonvolatile memory interface for burst read operations Nonvolatile semiconductor memory device
US 6625712 B2 US 6598190 B1 US 6597629 B1 US 6594177 B2 US 6587927 B2 US 6587364 B1 US 6584036 B2	6578129 6563732 6556490 6538932 6532174 6473356 6466504	6438670 6438036 6434658 6425116 6425062 6424556 6405160	6370078 6356302 6356503 6348774 6384774 6292427 6282131 6275902 6249901 6249901 6249471 6233197 6216180 61157576 6016273

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Apparatus for rejection diagnostics after organ transplants Method and apparatus for configurable memory emulation Nonvolatile semiconductor memory device Nonvolatile semiconductor memory device Timing scheme for memory arrays Nonvolatile semiconductor memory device Data processor with variable types of cache memories	Memory having direct strap connection to power supply Framework for constructing shared documents that can be collaboratively accessed by multi Nonvolatile semiconductor memory device Fast, dual ported cache controller for data processors in a packet switched cache coherent in Flash memory system Data processor and method of processing data in parallel Apparatus which detects lines approximating an image by repeatedly narrowing an area of th Dynamic random access memory device with sense amplifiers serving as cache memory inc Digital circuit design assist system for designing hardware units and software units in a desii Semiconductor memory device employing sense amplifier control circuit and word line contri Videotex terminal system using CRT display and binary-type LCD display Rule structure for insertion of new elements in a circuit design synthesis procedure Local in-device memory feature for electrically powered medical equipment Hold-type latch circuit with increased margin in the feedback timing and a memory device us Bitwise implementation mechanisms for a circuit design synthesis procedure Semiconductor memory device having a driving circuit provided in association with a high sp Integrated electric design system with automatic constraint satisfaction Method of and apparatus for detecting pattern defects by means of a plurality of inspecting u Image memory write control apparatus and exdure mapping apparatus Semiconductor memory with an improved nibble mode arrangement High-speed dual mode graphics memory Video terminal for use in graphics and alphanumeric applications Method and apparatus for generating a set of signals representing a curve Method and apparatus for generating a set of signals representing a curve Method and apparatus for generating a set of signals representing a curve Microfilm card and a microfilm reader with automatic stage positioning Referenced real-time ultrasonic image display Cache unit information replacement apparatus Cache unit information replacement apparatus Cache arrang	Parameter storage space allocation. Application specific integrated circuit chip has control block with defective memory register to
US 5970986 A US 5970240 A US 5959894 A US 5949715 A US 5923610 A US 5917752 A US 5848432 A	5808900 5781732 5644753 5644753 5644753 5640349 555555 552555 5479374 5479374 5479374 5479374 5479184 5479184 5479184 5479184 5479187 5046113 4945495 4875192 4875192 4875193 4886636 4688633 4688633 4688633 4431007 44311007	EP 647900 A1 US 7046561 B

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Read only memory instance for cor	Memory compiler for multi-instance Memory compiler units accessing n	Memory e.g. ROM characterization	Timing synchronization method in r	Automatic memory characterization	Display data encoding of signals re	Signal generation method for points
US 7035129 B	US 7031866 B US 20050060500 A	US 6738953 B	US 6282131 B	US 6249901 B	EP 191134 A	EP 175179 A